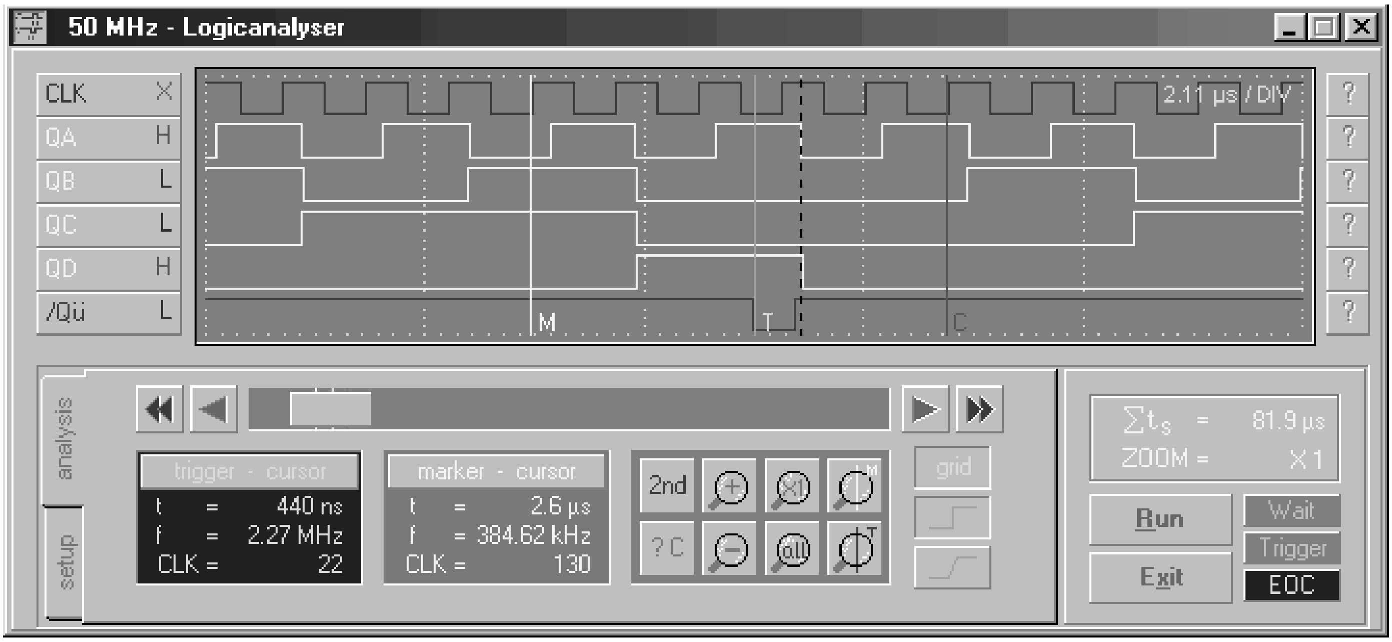
This professionally designed 16-channel logic analyser runs under Windows and is connected the PC's parallel printer port. It requires a minimum amount of hardware and costs a fraction of a comparable stand-alone instrument. A PC-controlled instrument, it offers ease of control and many ways of displaying measured signals.

software available on cd-rom
PC software 98-99

Design by K. Böhme

50-MHz logic analyser

First Prize, Germany



50 MHz - Logicanalyser

CLK X
QA H
QB L
QC L
QD H
/Qü L

2.11 µs / DIV

trigger - cursor
t = 440 ns
f = 2.27 MHz
CLK = 22

marker - cursor
t = 2.6 µs
f = 384.62 kHz
CLK = 130

$\sum t_s$ = 81.9 µs
ZOOM = X 1

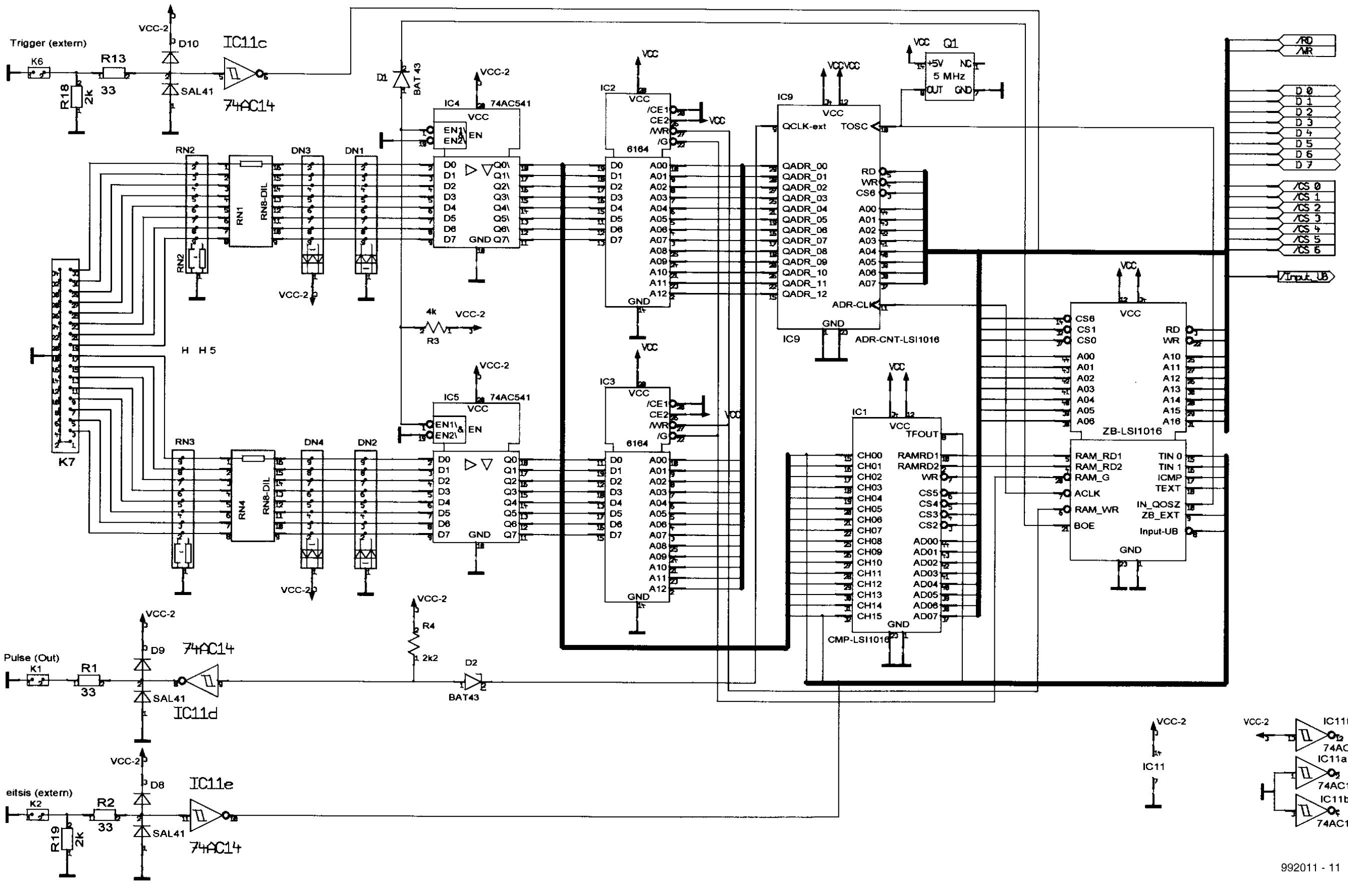
Main Specification

- Linked to computer via EP port (parallel printer interface)
- 16 channels (3 V or 5 V input swing)
- Sampling rate 1 kHz – 50 MHz (or by external clock up to 50 MHz)
- Adjustable pre-trigger from 1/8 to .7/8
- Triggering by CH00, CH15, adjustable bit pattern, or external
- Adjustable min. trigger pulsewidth from < =1, 4, 8, 15 samples
- Adjustable trigger edge
- Frequency output 10 Hz – 50 MHz
- Output level of frequency output 3 V or 5 V.

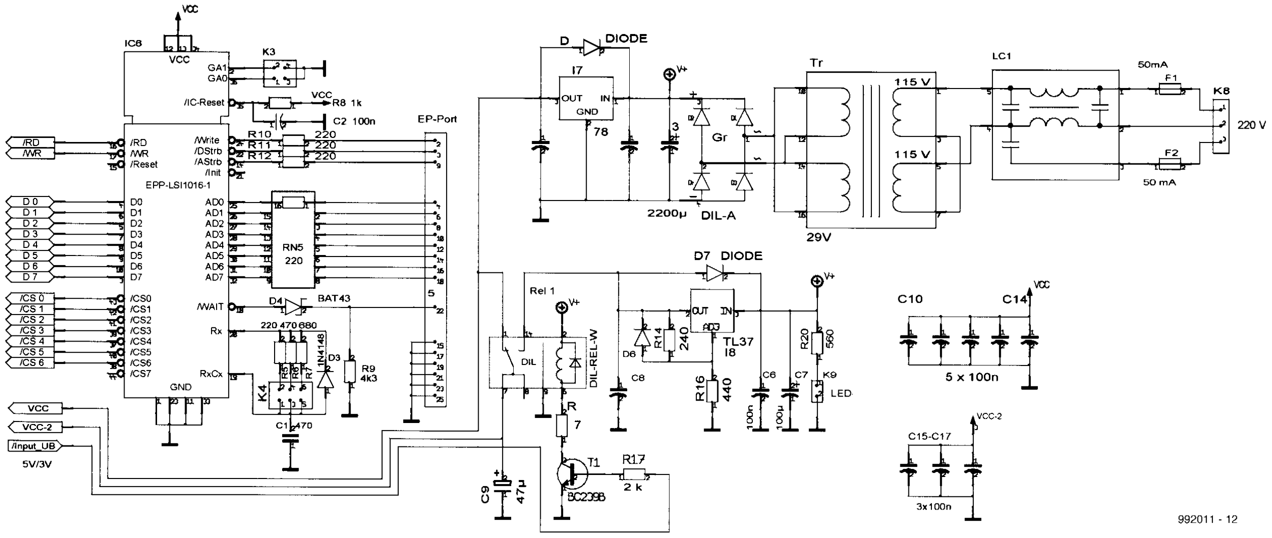
The instrument is controlled via a virtual front panel which appears on your PC screen. Apart from the customary user interface, the instrument offers all advantages of a PC running under Windows, including copying the readout into temporary storage, and post-processing of measured data by other Windows programs.

The hardware consists essentially of four Lattice FPGA devices type ispLSI1016 from Lattice. These devices appear prominently in the circuit diagrams in **Figures 1 and 2**. Circuit IC6 in Figure 2 is busy handling all data traffic on the EP port. The device number (3 for the analyser) may be set on two jumpers (K3), and the delay for the wait signal, on jumper K4. The IC receives an address write command to inform it about the chip select line to be set. The relevant IC is then addressed by the subsequent data read or write command.

The heart of the analyser is formed by IC10. This chip contains the entire process control system consisting of a presettable 12-bit up/down counter



Figures 1 and 2. In essence the hardware of the Logic Analyser consists of four ispLSI chips from Lattice.



with decoding logic. At the start of a measurement, the pre-trigger value is loaded, and this is counted down to zero. Once at 00, the decoding logic disables itself, reverts the count direction, and then enables the trigger control. If a trigger pulse arrives at that instant, the counter is reloaded with the pre-trigger value, and counts up until an overflow is produced. It then disables itself, as well as the RAMs and their address counters. This concludes the measurement, and the data stored in the RAMs may be read by the system.

The same IC also contains the input multiplexers for the timebase, the trigger source selection logic, and the counter for the minimum trigger pulsewidth.

The control signals supplied by this subcircuit are:

- RAMRD_1:	read RAM1
- RAMRD_2:	read RAM2
- RAM_G:	output enable for both RAMs

- ACLK: clock signal for address counter
- RAM_WR: write signal for both RAMs
- BOE: output enable for input drivers IC4/IC5
- Input_UB: goes to Re1 and there controls the voltage switchover for the input and output drivers (IC4, IC5 and IC11).

Circuit IC9 contains the dividers for the variable output frequencies, two multiplexers for their selection, and a 12-bit counter which acts as an address counter for the two RAMs.

IC1 contains an 8-bit multiplexer for the reading of the two RAMs, the storage registers for the set trigger word, and a comparator which pulls the TFOUT output logic high when the levels at the analyser inputs match those set up in the trigger word.

Circuit IC2 and IC3 are fast RAMs with a capacity of 8 kBytes each. The program uses about 4 kBytes, an extension to 8 kBytes is already supported by the PCB layout.

Circuits IC4 and IC5 are input drivers between the inputs and the RAMs. IC11 acts as a driver for the signals at the output sockets, and at IC10. Relay Re1 allows all driver ICs to work with 3.5 V or 5 V logic swing. Both supply voltages are provided by IC7 and IC8.

Software functions and documentation

The 32-bit control program (written in Visual BASIC V5) takes care of all hardware control and also provides an easy way of browsing the 4-kByte memory area. Further functions include setting two marker lines, outputting measurement values, and setting up trigger points and markers using at the mouse cursor location. You can jump to the marker lines by means of a mouse click.

Zooming is possible via ‘buttons’, while an area to be examined in detail may be enlarged by drawing a rectangle with the mouse.

Program settings as well as entire data files may be stored complete with comment, for retrieval at a later time.

For documentation purposes, the contents of the active window may be copies into temporary storage, from which it may be loaded by other programs including word processors.

All channels may be displayed in a certain colour and they may be given a name. To make sure the control elements and the actual data display are quickly available without having to jump between partly obscured windows, the windows are divided between two register cards (tabs), and displayed as fixed elements in a separate window which also contains the data display.

Apart from descriptions of the circuit diagram, the circuit operation and program installation (in a Word file), the documentation as supplied by the author also includes the actual circuit diagrams, the copper track layout and component mounting plan of the double-sided printed circuit board (in a TIFF file), as well as all source code files and sample data files which should enable you to check the operation of the program.

The complete set of documentation files and program files covering the use and installation of the program may be found on a CD-ROM which contains a large number of winning entries from our 1998 Software Design Contest. This CD-ROM will be available early January 1999. More details will be given in the forthcoming February 1999 issue of *Elektor Electronics*.

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